

## Description

This test measures the accuracy of the cell voltage measurement circuits of the X3100. In the test, a known voltage is applied across each cell input of the X3100. The analog output voltage of the X3100 is measured for each cell. This value is compared to the input voltage. The collected data includes the values from three devices from three different lots. The data also includes tests at 0°C, 25°C and 50°C.

## Test Setup

For this test, Vcc was held at 16V to prevent the device entering the sleep mode when testing cell voltages below 2V. In the test 4V was applied to all cells, except the cell being measured. The voltage was applied at 10mV intervals over four ranges. These input ranges were 1.5 to 1.7V, 2.5 to 2.7V, 3.5 to 3.7V and 4.0 to 4.2V.

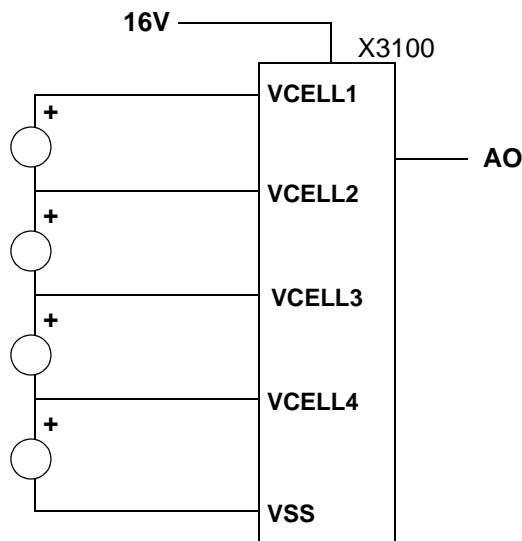


FIGURE 1. CELL VOLTAGE MEASUREMENT

For each cell and each applied voltage the output was recorded. This involves the changing of the analog multiplexer setting in the X3100. In gathering the data with this test, the output was sample. This procedure was used to reduce the effect of external noise on the test environment.

## Results

The data for this test is available in raw form in an Excel spreadsheet. This spreadsheet includes data for each device, data for each lot, and data for all devices. Each set of data includes results for the three temperature settings and the four gain settings. The data was copied to other files for the purposes of generating graphs.

The result summaries show the output error as a percentage. This error is provided for each of 3 lots as well as the combined data. Data is averaged, and standard deviation computed, from samples taken at three temperatures 0°C, 25°C and 50°C.

On the following charts, absolute error is the Output minus the Input, while the percent error is calculated as follows:

$$\text{Error} = \frac{\text{Output} - \text{Input}}{\text{Input}}$$

## Overall Performance

The following set of graphs shows the performance of the X3100 over temperature and across three lots of three devices. The graphs will show the basic input/output curve, raw error, and error after correction for offset and gain.

The below data shows that the X3100 output is accurate, with 3 standard deviations, to better than 2.5% error across all measured voltages. It also shows that over the key range of 2.5 to 4.2V, accuracies of better than 1% can be expected. These accuracies are not dependent on any calibration factors.

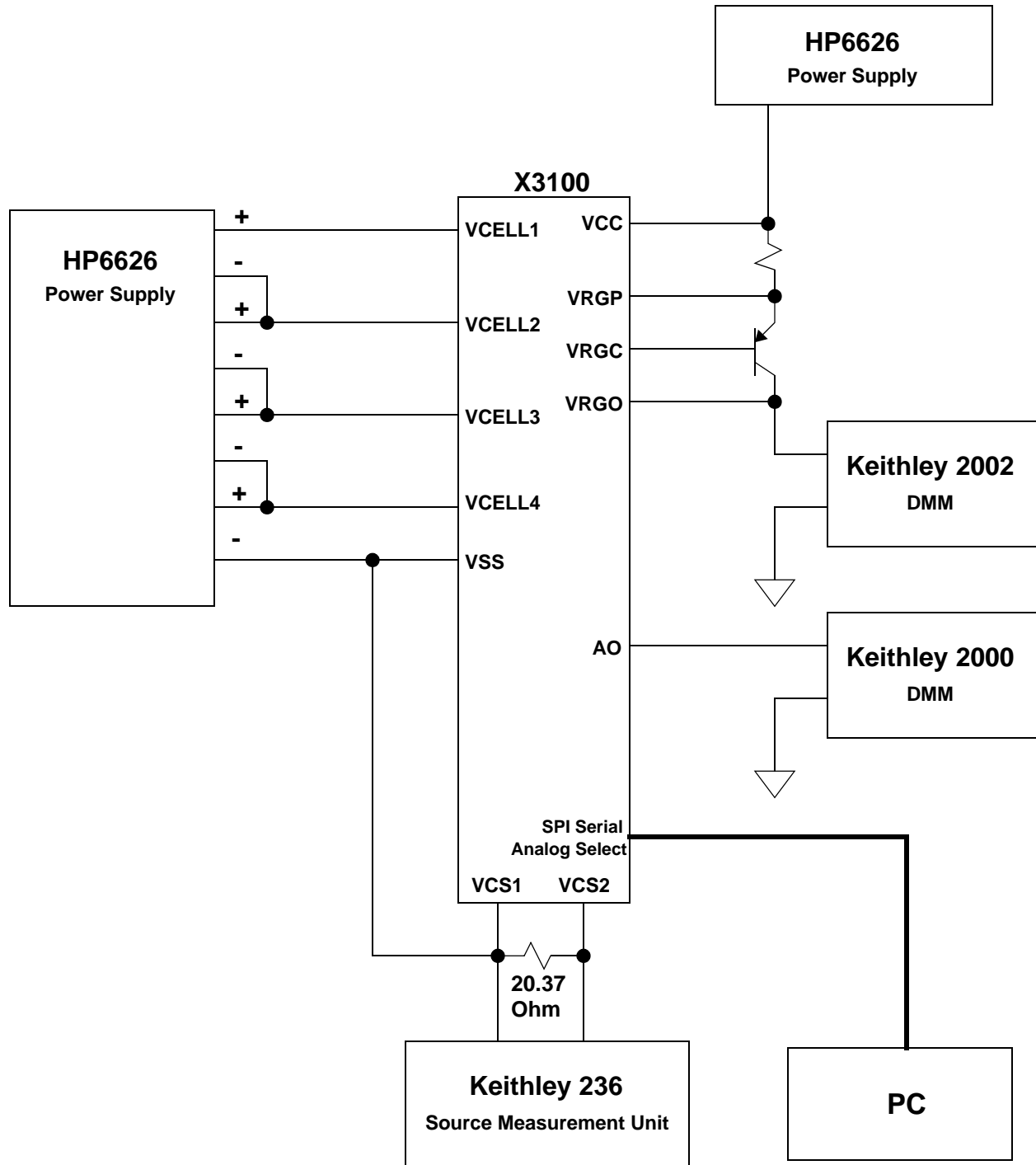


FIGURE 1. CHARACTERIZATION TEST SETUP

Lot 1

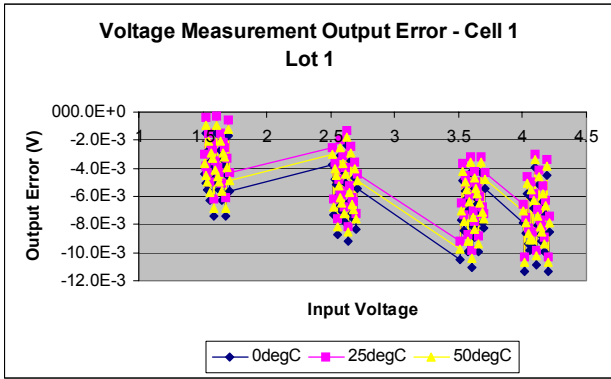


FIGURE 2A.

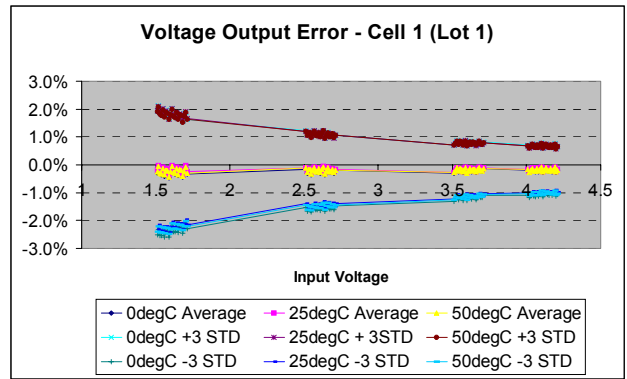


FIGURE 2B.

FIGURE 2. INPUT TO OUTPUT VOLTAGE ERROR - CELL 1

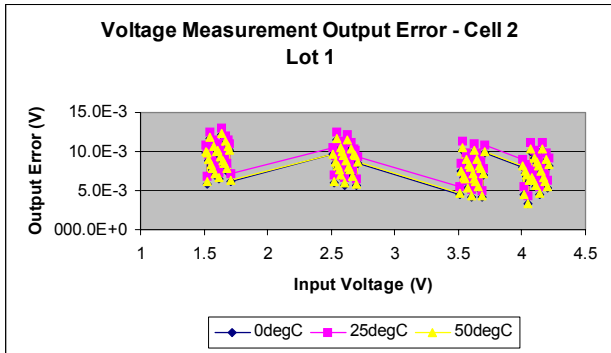


FIGURE 3A.

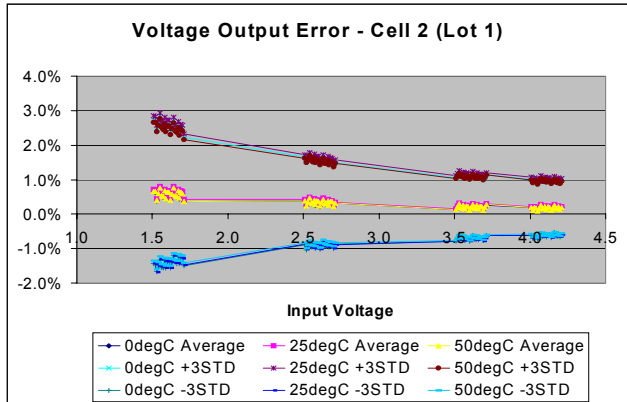


FIGURE 3B.

FIGURE 3. INPUT TO OUTPUT VOLTAGE ERROR - CELL 2

Lot 1 continued

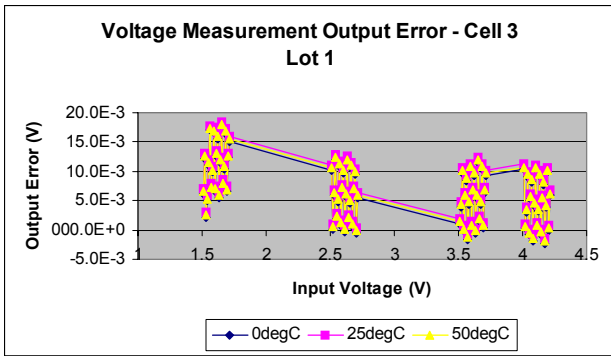


FIGURE 4A.

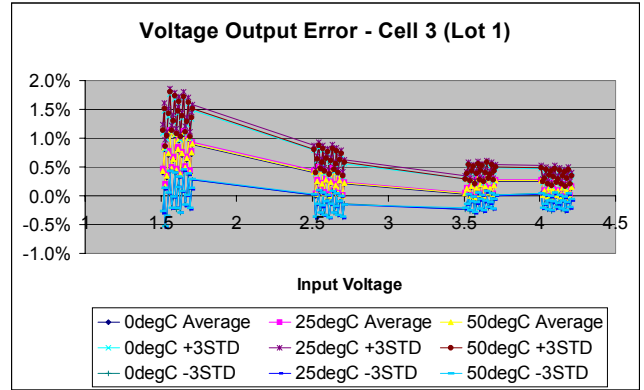


FIGURE 4B.

FIGURE 4. INPUT TO OUTPUT VOLTAGE ERROR - CELL 3

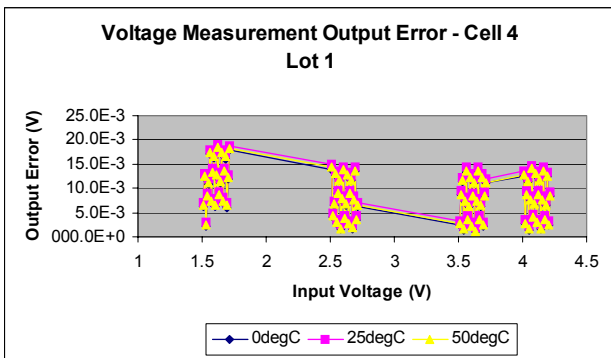


FIGURE 5A.

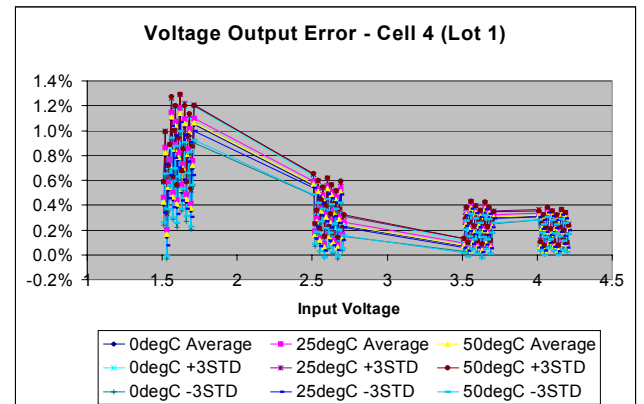


FIGURE 5B.

FIGURE 5. INPUT TO OUTPUT VOLTAGE ERROR - CELL 4

Lot 2

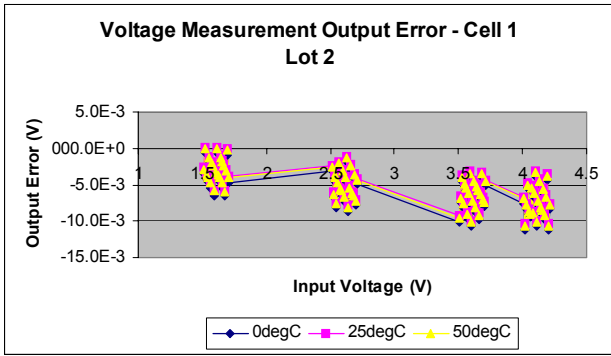


FIGURE 6A.

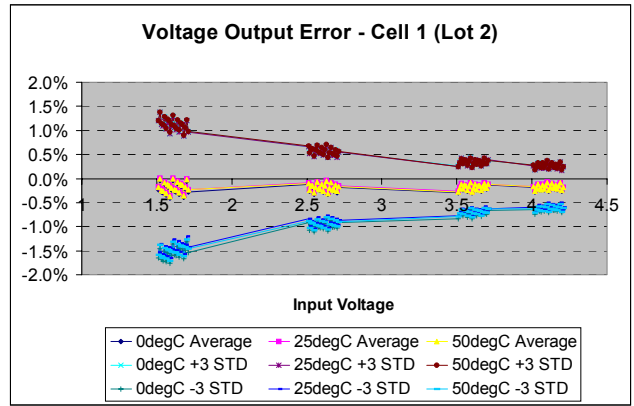


FIGURE 6B.

FIGURE 6. INPUT TO OUTPUT VOLTAGE ERROR - CELL 1

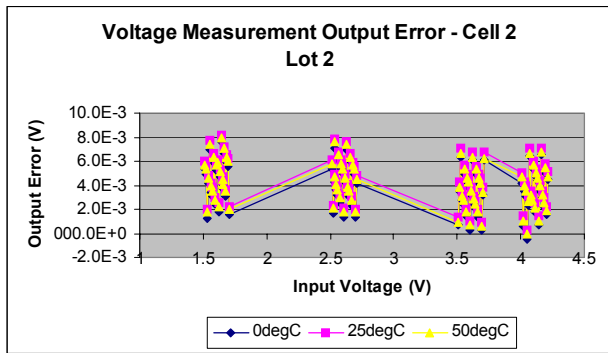


FIGURE 7A.

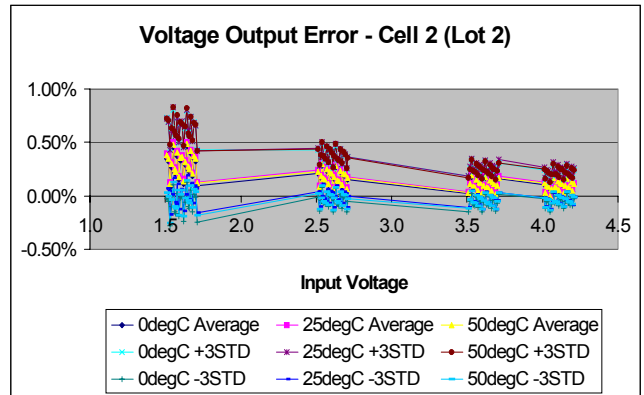


FIGURE 7B.

FIGURE 7. INPUT TO OUTPUT VOLTAGE ERROR - CELL 2

Lot 2 (Continued)

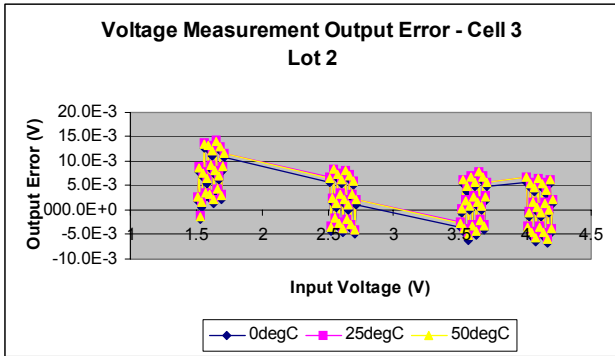


FIGURE 8A.

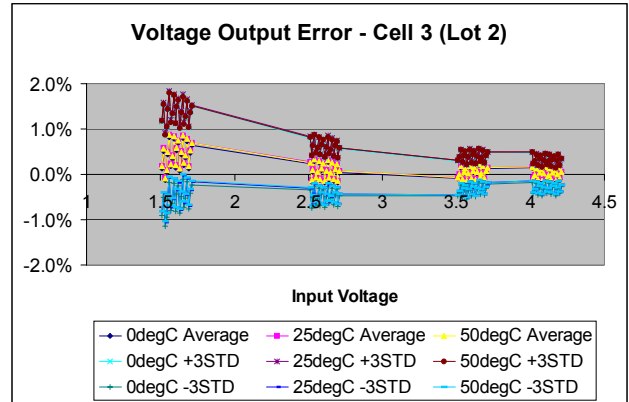


FIGURE 8B.

FIGURE 8. INPUT TO OUTPUT VOLTAGE ERROR - CELL 3

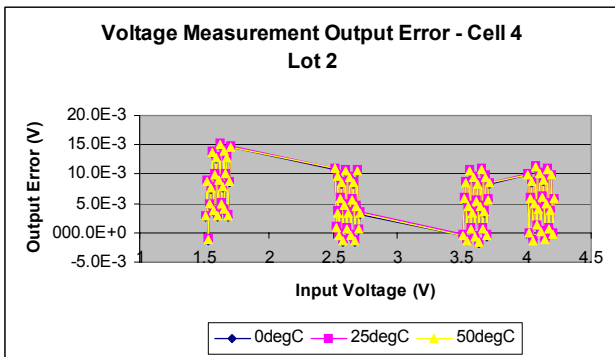


FIGURE 9A.

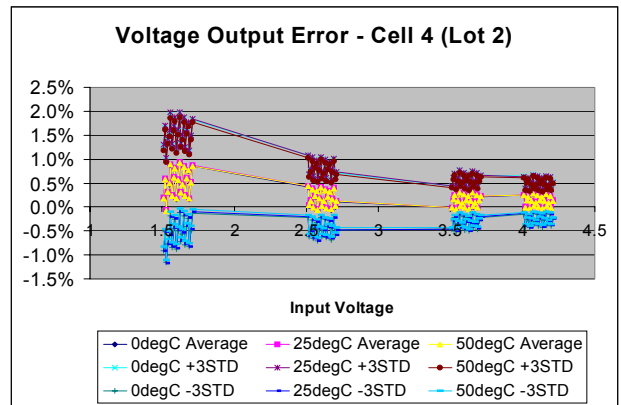


FIGURE 9B.

FIGURE 9. INPUT TO OUTPUT VOLTAGE ERROR - CELL 4

Lot 3

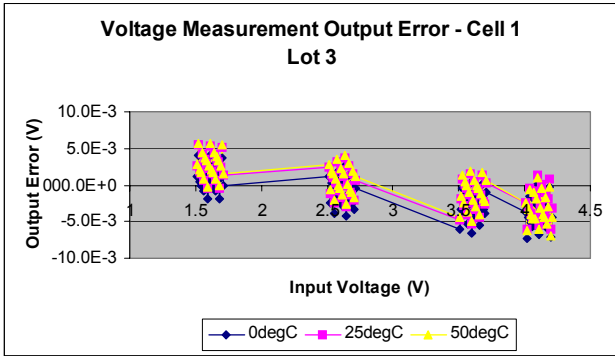


FIGURE 10A.

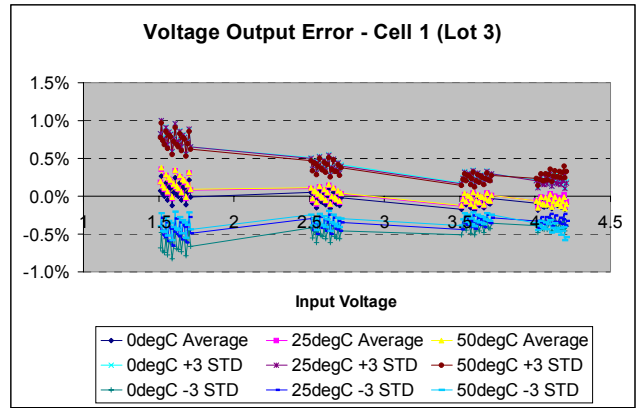


FIGURE 10B.

FIGURE 10. INPUT TO OUTPUT VOLTAGE ERROR - CELL 1

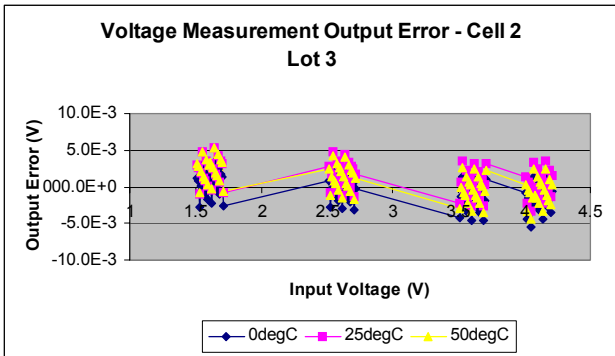


FIGURE 11A.

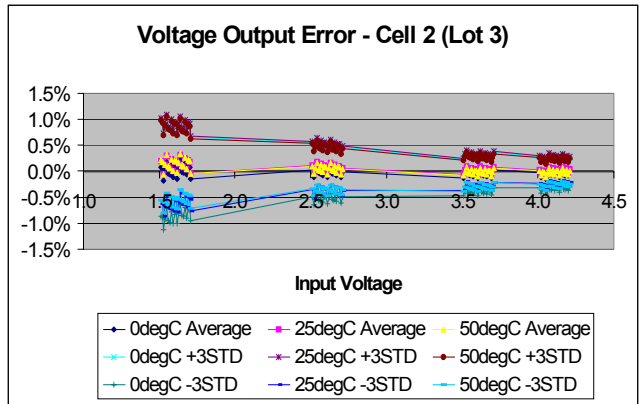


FIGURE 11B.

FIGURE 11. INPUT TO OUTPUT VOLTAGE ERROR - CELL 2

Lot 3 (Continued)

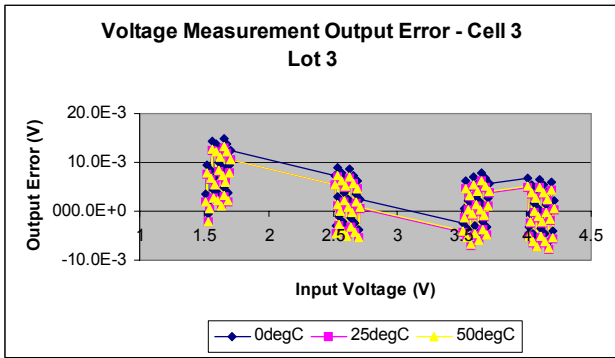


FIGURE 12A.

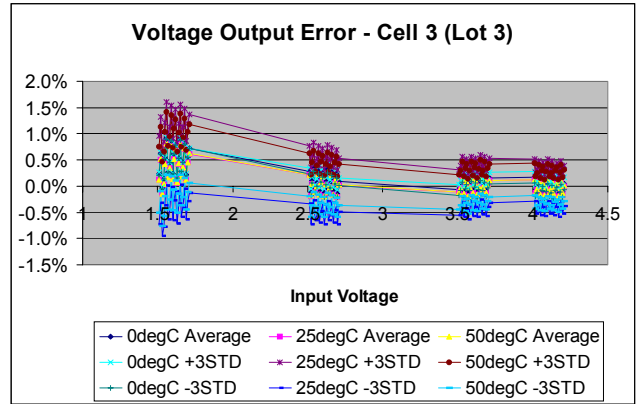


FIGURE 12B.

FIGURE 12. INPUT TO OUTPUT VOLTAGE ERROR - CELL 3

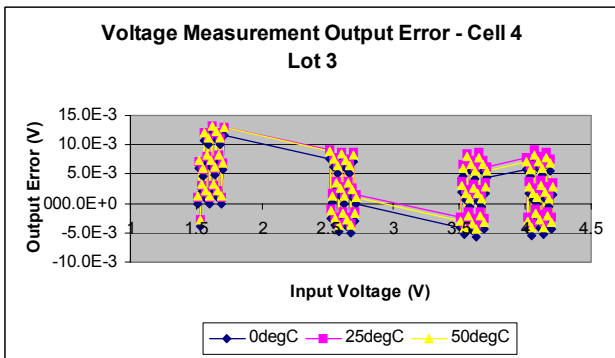


FIGURE 13A.

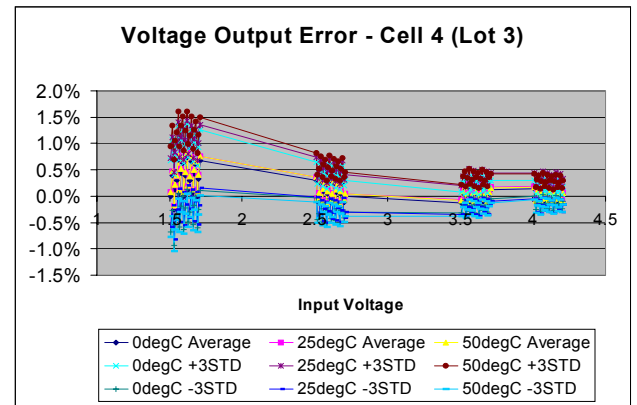


FIGURE 13B.

FIGURE 13. INPUT TO OUTPUT VOLTAGE ERROR - CELL 4



Combine All Lots

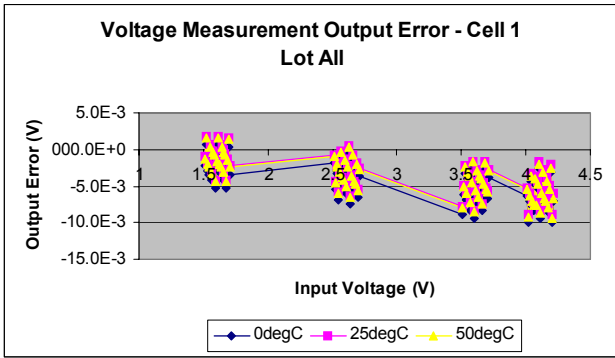


FIGURE 14A.

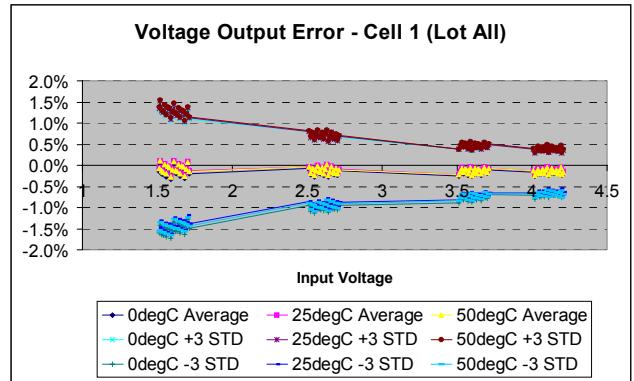


FIGURE 14B.

FIGURE 14. INPUT TO OUTPUT VOLTAGE ERROR - CELL 1

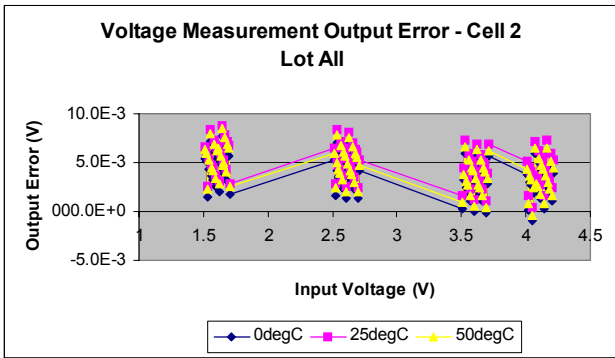


FIGURE 15A.

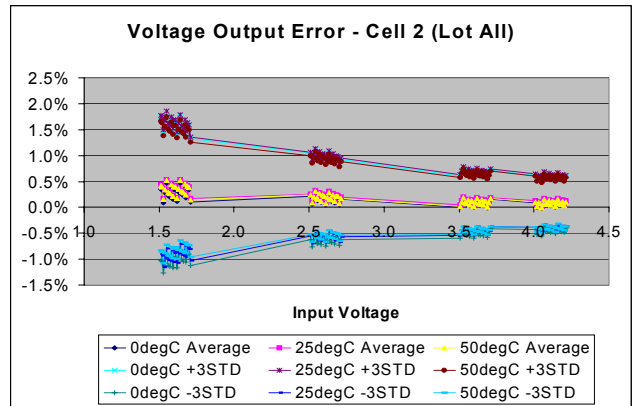


FIGURE 15B.

FIGURE 15. INPUT TO OUTPUT VOLTAGE ERROR - CELL 2

Combine All Lots (Continued)

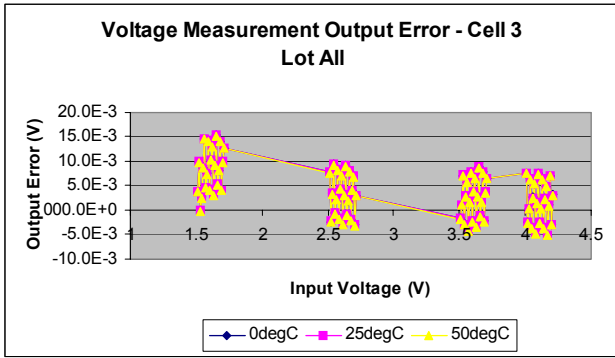


FIGURE 16A.

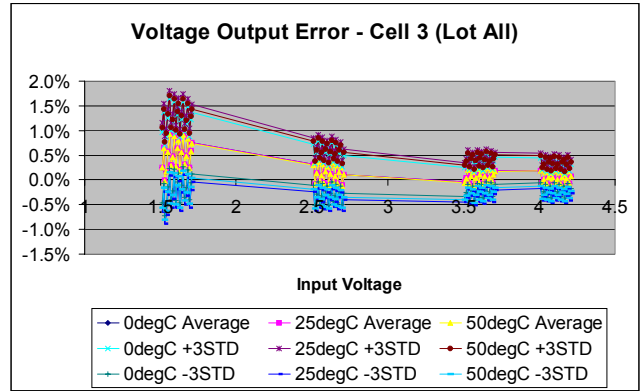


FIGURE 16B.

FIGURE 16. INPUT TO OUTPUT VOLTAGE ERROR - CELL 3

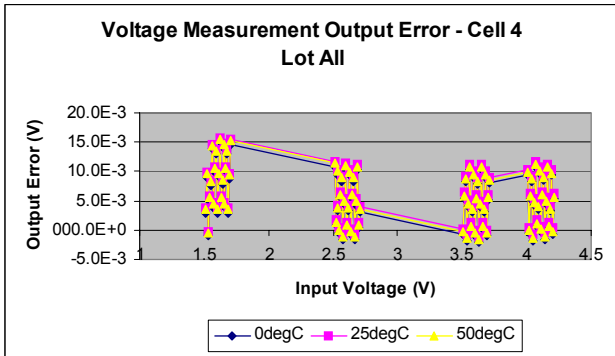


FIGURE 17A.

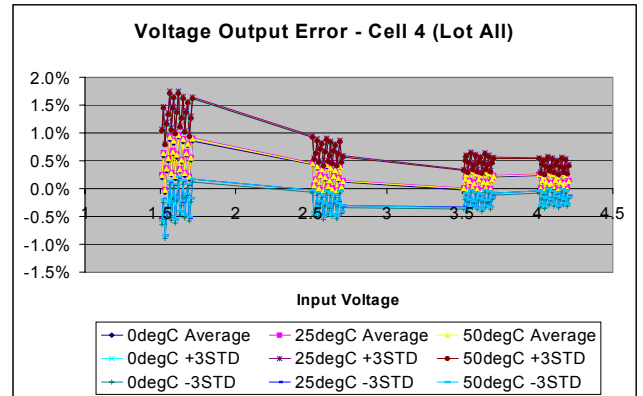


FIGURE 17B.

FIGURE 17. INPUT TO OUTPUT VOLTAGE ERROR - CELL 4

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